REMARKS

In an Office Action mailed on December 28, 2005, claims 1, 2 and 3 were rejected under 35 U.S.C. § 102(b) as being anticipated by Leonida; claims 4-6, 8, 9, 12-14, 18-21, 23 and 24-28 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Leonida in view of Silvestri and Dvorak; and claims 10, 11, 15, 16, 17 and 22 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Dvorak in view of Leonida. The §§ 102 and 103 rejections are addressed below.

§§ 102 and 103 Rejections of Claims 1-9:

As amended, the system of independent claim 1 includes a locked loop circuit to provide an indication of a phase difference between an input signal and an output signal. The system includes a processor that is coupled to the locked loop circuit to control the locked loop circuit based on the indicated phase difference and perform at least one other function in the system that is not related to the control of the locked loop circuit.

Leonida fails to teach or suggest the limitations of amended independent claim 1. In this regard, Leonida discloses a duty cycle controller, or fine delay element 182, that has fine delay select bus 162 that is written by a master processor 116. In this regard, the master processor 116 selects a duty cycle for the output signal (called "MMCLK") of the fine delay element 182 by writing the appropriate value to the fine delay select bus 162. Leonida does not, however, teach or even suggest that the fine delay element 182 provides an indication of a phase difference between an input signal and an output signal, such that the master processor 116 controls the fine delay element 182 based on this indication. Thus, not only does Leonida fail to teach or suggest the claimed invention, there is no suggestion or motivation to modify Leonida (in view of Silvestri or Dvorak, for example) to derive the claimed invention, as there is no suggestion or motivation shown in the cited art to modify Leonida's fine delay element 182 so that the element 182 is controlled via a feedback loop between the fine delay element 182 and the master processor 116. Therefore, allowance of amended independent claim 1 is requested.

Claims 2-9 are patentable for at least the reason that these claims depend from an allowable claim.

§ 103 Rejections of Claims 10-15:

As amended, the locked loop circuit of independent claim 10 includes an interface that is accessible by a processor to control the locked loop circuit to adjust a timing between an input clock signal and an output clock signal based on a phase difference that is indicated by a phase detector of the locked loop circuit.

Although the phase detector 310 of Dvorak may indicate a phase difference between input and output clock signals, there is no teaching or suggestion in Dvorak relating to the control of the phase locked loop by a processor to control a locked loop circuit. Leonida discloses a fine delay select bus 162 that is written to by a processor 116 but fails to teach or suggest providing any type of indication to the processor 116 for purposes of controlling the fine delay element 182. Therefore, there is no suggestion or motivation in the cited references to modify Dvorak so that its circuitry is controlled by a processor to adjust a timing relationship between input and output clock signals. As such, Applicant requests withdrawal of the § 103 rejection of independent claim 10.

Claims 11-15 are patentable for at least the reason that these claims depend from an allowable claim.

§ 103 Rejections of Claims 16-23:

The method of independent claim 16, as amended, recites using a processor to control a locked loop circuit based on a timing indication provided by the locked loop circuit and perform at least one other function that is not related to the control of the locked loop circuit.

Contrary to the limitations of amended independent claim 16, the hypothetical combination of Dvorak and Leonida fails to teach or suggest all claim limitations. In this regard, this hypothetical combination fails to teach or suggest the act of using a processor to control a locked loop circuit based on a timing indication from the locked loop circuit. More specifically, Dvorak discloses a phase detector 310 that may arguably provide an indication of a timing between input and output signals but fails to teach or suggest the feedback of this indication to a processor for purposes of controlling a locked loop circuit. Leonida discloses a one way communication from the master processor 116 to the time delay element 182 for purposes of the processor 116 setting the duty cycle produced by the fine delay element 182, but Leonida fails to teach or suggest any feedback that is provided by the fine delay element 182 to the main processor 116, such as an

indication of a timing, for example. Thus, for at least the reason that the hypothetical combination of Dvorak and Leonida fails to teach or suggest all of the limitations of amended independent claim 16, withdrawal of the § 103 rejection of this claim is requested.

Claims 17-23 are patentable for at least the reason that these claims depend from an allowable claim.

§ 103 Rejections of Claims 24-28:

As amended, the article of independent claim 24 includes a computer accessible storage medium that stores instructions to, when executed, cause a processor to receive an indication of a timing of a locked loop circuit and control the locked loop circuit.

See discussions of independent claims 10 and 16 above. In particular, the hypothetical combination of Dvorak, Leonida and Silvestri fails to teach or suggest all of the limitations of amended independent claim 24 for at least the reason that none of these references teach or suggest a processor that executes instructions to cause the processor to receive an indication of a timing from the locked loop circuit. The only communication that is disclosed in any of these three references is the writing of the duty cycle information from the main processor 116 of Leonida to the fine delay element 182. There is, however, no teaching or suggestion in any of the references relating to a processor that receives an indication of a timing of the locked loop circuit. As such, withdrawal of the § 103 rejection of independent claim 24 is requested.

Claims 25-28 are patentable for at least the reason that these claims depend from an allowable claim.

CONCLUSION

In view of the foregoing, withdrawal of the §§ 102 and 103 rejections and a favorable action in the form of a Notice of Allowance are requested. The Commissioner is authorized to charge any additional fees or credit any overpayment to Deposit Account No. 20-1504 (ITL.0550US).

Respectfully submitted,

Date: January 12, 2006

Fred G. Pruner, Jr., Registration No. 40,779
TROP, PRUNER & HU, P.C.
8554 Katy Freeway, Suite 100
Houston, TX 77024
(713) 468-8880
(713) 468-8883 FAX

Attorney for Intel Corporation